Abstract Submitted
for the 4CF06 Meeting of
The American Physical Society

Electron transport in laterally confined phosphorus δ-layers in silicon[1] S.J. ROBINSON, J.R. TUCKER, University of Illinois at Urbana-Champaign, T.-C. SHEN, Utah State University — Carrier transport in 1D semiconductor structures has not been much studied experimentally because of the difficulty of confining dopant atoms in a quasi-1D configuration in a crystal. In the past few years we have developed a UHV-STM-based fabrication scheme to create 2D nanoscale patterns buried in crystalline silicon. By selectively desorbing H from a Si surface and dosing the dangling bonds with PH_3, we can create laterally confined conductive P δ-layers with widths on the order of 10 nm. These nanowires are connected to arrays of As-implanted contacts for transport characterization. Electrical measurements at cryogenic temperatures show ohmic behavior and magnetoconductance in accordance with weak localization theory. In addition, by lowering the temperature continuously, we find a clear 2D to 1D transition as the phase coherence length approaches the wire width. In 1D, the nanowire resistance becomes independent of temperature, indicating a saturation of the phase coherence and thermal lengths due to inelastic boundary scattering in the wire. Large-scale integration of δ-layer devices and potential 3D architectures will become possible by employing the UHV-photolithography currently under development.

[1]This work is supported by NSF-NIRT under Grant No. CCF-0404208.

Stephen Robinson
University of Illinois at Urbana-Champaign

Date submitted: 11 Sep 2006 Electronic form version 1.4