

Abstract Submitted
for the APR16 Meeting of
The American Physical Society

A Simulation of the Front End Signal Digitization for the ATLAS Muon Spectrometer thin RPC trigger upgrade project. XIANGTING MENG, JOHN CHAPMAN, DANIEL LEVIN, TIESHENG DAI, JUNJIE ZHU, BING ZHOU, Univ of Michigan - Ann Arbor, UM ATLAS GROUP TEAM — The ATLAS Muon Spectrometer Phase-I (and Phase-II) upgrade includes the BIS78 muon trigger detector project: two sets of eight very thin Resistive Place Chambers (tRPCs) combined with small Monitored Drift Tube (MDT) chambers in the pseudorapidity region $1 < |\eta| < 1.3$. The tRPCs will be comprised of triplet readout layer in each of the eta and azimuthal phi coordinates, with about 400 readout strips per layer. The anticipated hit rate is 100-200 kHz per strip. Digitization of the strip signals will be done by 32-channel CERN HPTDC chips. The HPTDC is a highly configurable ASIC designed by the CERN Microelectronics group. It can work in both trigger and trigger-less modes, be readout in parallel or serially. For Phase-I operation, a stringent latency requirement of 43 bunch crossings (1075 ns) is imposed. The latency budget for the front end digitization must be kept to a minimal value, ideally less than 350 ns. We conducted detailed HPTDC latency simulations using the Behavioral Verilog code from the CERN group. We will report the results of these simulations run for the anticipated detector operating environment and for various HPTDC configurations.

Xiangting Meng
Univ of Michigan - Ann Arbor

Date submitted: 06 Jan 2016

Electronic form version 1.4