

Abstract Submitted
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The Development of FPGA-Based Pseudo-Iterative Clustering Algorithms ELIZABETH DRUEKE, WADE FISHER, PAWEL PLUCINSKI, Department of Physics and Astronomy, Michigan State University — The Large Hadron Collider (LHC) in Geneva, Switzerland, is set to undergo major upgrades in 2025 in the form of the High-Luminosity Large Hadron Collider (HL-LHC). In particular, several hardware upgrades are proposed to the ATLAS detector, one of the two general purpose detectors. These hardware upgrades include, but are not limited to, a new hardware-level clustering algorithm, to be performed by a field programmable gate array, or FPGA. In this study, we develop that clustering algorithm and compare the output to a Python-implemented topoclustering algorithm developed at the University of Oregon. Here, we present the agreement between the FPGA output and expected output, with particular attention to the time required by the FPGA to complete the algorithm and other limitations set by the FPGA itself.

Elizabeth Drueke
Department of Physics and Astronomy, Michigan State University

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