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Results of FE65-P2 Stability Tests for the High Luminosity LHC **Upgrade** KATHERINE DUNNE, Lawrence Berkelev National Lab, ATLAS COL-LABORATION — The high luminosity upgrade of the LHC sets an imperative for readout technology capable of handling the consequences of higher particle interaction rates. Increased luminosity exists hand-in-hand with unprecedented levels of radiation and the need for exceptional logic density to store hit information during a trigger latency period on the order of 10  $\mu$ s. The RD53 collaboration has developed specifications for the new generation of hybrid pixel readout chips to be included in the ATLAS and CMS Phase 2 upgrades. The FE65-P2 is a test readout chip fabricated on 65 nm CMOS technology that prototypes these design variants. Objectives of FE65-P2 include demonstrating the novel process of isolated analog front ends embedded in a digital design, known as "analog islands in a digital sea." In addition, the innermost layer of the pixel detector in the upgraded ATLAS experiment will reach doses approaching 1 Mrad per run, and a single FE65-P2 should be tolerant to a lifetime dose near 500 Mrad. This talk will cover the test results of FE65-P2 calibration and stability. The experience gained from such tests will advise the development of RD53A, a large format readout chip to be fabricated in early 2017.

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