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Improvement of Event Synchronization in the ATLAS Pixel Readout Development LOGAN ADAMS[1], University of Washington, ATLAS COLLABORATION — As the LHC continues in Run2, the B-Layer still uses the Atlas-SiROD Pixel readout system initially developed for Run 1. The higher luminosity occurring during Run 2 results in higher occupancy causing increased desynchronization errors in the Pixel Readout. In order to ensure lasting operation of the B-Layer until it is replaced after Run 3, changes were made to the firmware and software to add debug capabilities to identify when the errors are crossing certain thresholds and change the internal control logic accordingly. These features also allow for better debugging of the Event Counter Reset addition to the firmware. This talk will focus on the features implemented and measurements to demonstrate the positive impact on the Pixel DAQ system. A Pixel front-end chip emulator which can be used for readout system development beyond Run 3 will also be discussed.

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