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Design of a time-to-digital converter (TDC) ASIC for the Phase-II upgrade of the ATLAS muon spectrometer YU LIANG, University of Sci. and Tech. of China, University of Michigan, ATLAS COLLABORATION — To cope with a large amount of data and high event rate expected from the planned High-Luminosity LHC (HL-LHC) upgrade in pp collisions at $\sqrt{s}=13$ TeV with the ATLAS detector, the ATLAS monitored drift tube (MDT) readout electronics will be replaced. In addition, the MDT detector will be used at the first-level trigger to improve the muon transverse momentum resolution and reduce the overall trigger rate. A new trigger and readout system has been proposed. A new time-to-digital converter (TDC) ASIC is needed at the frontend board to digitize the discriminated muon drift time signal. We also designed a demonstrator TDC prototype and studied its timing, latency and power consumption. In this talk, we will present the design and simulation results of a TDC with all needed features included. In addition, we will present the performance of the demonstrator TDC ASIC that we built.

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