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Design and performance of the Trigger Data Serializer ASIC for the Phase-I upgrade of the ATLAS forward muon spectrometer XIONG XIAO, University of Michigan, ATLAS COLLABORATION — The present small wheel muon detector at ATLAS will be replaced with a New Small Wheel (NSW) detector to handle the increase in data rates and harsh radiation environment expected at the LHC. Resistive Micromegas and small-strip Thin Gap Chambers (sTGC) will be used to provide both trigger and tracking primitives in pp collisions at $\sqrt{s} = 13$ TeV with the ATLAS detector. Signals from the sTGC pad and strip detectors will be read out by the Amplifier Shaper Discriminator (ASD) ASIC, and then collected by the Trigger Data Serializer (TDS) ASIC before being transmitted via twinax cables to other circuits located on the rim of the NSW detector. In order to reduce the output data rate, the TDS ASIC also performs pad-strip matching and only strips underneath certain pads will be read out. The large number of input channels (128 differential input channels), short time available to prepare and transmit trigger data (¡100 ns), high speed output data rate (4.8 Gbps), harsh radiation environment (about 300 kRad), and low power consumption (¡1 W) all impose great challenges for the design of this ASIC using the IBM 130 nm CMOS process. We present the design and performance of the TDS ASIC.

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