Abstract Submitted
for the APR21 Meeting of
The American Physical Society

The ETROC Project: ASIC Development for CMS MTD Endcap Timing Layer (ETL) Upgrade ZHENYU YE, University of Illinois at Chicago, CMS COLLABORATION — The Endcap Timing Readout Chip (ETROC), being developed for the CMS Endcap Timing Layer (ETL) for high luminosity LHC (HL-LHC), is presented. Each endcap will be instrumented with a two-disk system of MIP-sensitive LGAD silicon devices to be read out by ETROCs for precision timing measurements with time resolution down to 30 ps level. The ETROC is designed to handle a 1616 pixel cell matrix, each pixel cell being 1.3×1.3 mm^2 to match the LGAD sensor pixel size. The design of ETROC as well as prototype testing results are presented.

Zhenyu Ye
University of Illinois at Chicago

Date submitted: 11 Jan 2021 Electronic form version 1.4