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FPGA-based firmware implementation of a missing transverse momentum algorithm for the CMS Phase-2 Level-1 trigger JIEUN HONG, Kyungpook Natl Univ, CMS COLLABORATION — The high-luminosity upgrade of the CERN Large Hadon Collider (HL-LHC) will enable a factor of ten increase in the total dataset collected by the CMS experiment, maximizing the potential for the discovery of new physics. While the increased instantaneous luminosity will bring this significant advantage, it also requires improved capabilities of the CMS detector performance. The CMS Level-1 trigger will be significantly expanded during the Phase-2 upgrade to allow for more efficient data collection. The Level-1 correlator trigger will become the main engine of the trigger system, performing particle-flow (PF) reconstruction, which reconstructs physics objects by combining signals collected by all subdetectors. These PF objects are passed to a second-stage FPGA for further processing into higher-level objects. This work describes the firmware implementation of a missing transverse momentum algorithm, developed using Xilinx Vivado high-level synthesis, including emulation results with the prototype trigger board.

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