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Nanoelectronics and Plasma Processing — The Next 15 Years and Beyond

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The number of transistors per chip has doubled every 2 years since 1959, and this doubling will continue over the next 15 years as transistor sizes shrink. There has been a 25 million-fold decrease in cost for the same performance. There are now as many as 1.5 billion transistors on-chip, with gate lengths as small as 37 nm (120 atoms) and oxide thicknesses as small as 1.5 nm (5 atoms). The smallest working transistor has a 5 nm (17 atoms) gate length, close to the limiting gate length, from simulations, of about 4 nm. Plasma discharges are used to fabricate hundreds of billions of these nano-size transistors on a silicon wafer. These discharges have evolved from a first generation of "low density" reactors capacitively driven by a single source, to a second generation of "high density" reactors (inductive and electron cyclotron resonance) having two rf power sources, in order to control independently the ion flux and ion bombarding energy to the substrate. A third generation of "moderate density" reactors, driven capacitively by one high and one low frequency rf source, is now widely used. Recently, triple frequency and combined dc/dual frequency discharges have been investigated, to further control processing characteristics, such as ion energy distributions, uniformity, and plasma etch selectivities. There are many interesting physics issues associated with these discharges; an example of electromagnetics effects will be described. Beyond the 4 nm transistor limit lies a decade of further performance improvements for conventional nanoelectronics, and beyond that, a dimly-seen future of spintronics, single-electron transistors, cross-bar latches, and molecular electronics.