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Plasma Etching of Nano-Scale Features

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As the technology moving to deep nanometer regime, patterning nano-scale semiconductor features with precision imposes many new challenges for plasma etching. Two of the challenges are evidently critical. One of the challenges is that as the sizes of nano-scale features shrinking down to the sub-10nm regime, plasma etching seems to approach to its 'limits' in unprecedented ways. For instance, one may face the question of what is the smallest hole can be actually etched by plasmas. Another challenge is the precision controllability of nano-scale feature pattern transferring as the features sizes, masks materials and thickness being all shrinking down to the molecular cluster dimensions. In this paper, we summarize the recent results of studying plasma etching of true nano-scale features using variety of nano-scale patterns and masks, diblock copolymer (similar to resist) self assembled nano holes and lines and self-assembled organosilicate (similar to silicon oxide) nano patterns. Using samples patterned with arrays of nano hole or nano line dimensions in the range from 25nm down to sub-10nm, we studied plasma etching characteristics and challenges for transferring nano-scale patterns into different materials (silicon, and silicon dioxide) in different plasma chemistries and process conditions. By varying the dimensions and thickness of masks, the characteristics of aspect ratio dependence vs. 'true' etching limits due to the sizes of sub-25nm nano-scale features were studied. The impacts and challenges of mask selectivity and line edge roughness (LER) to transfer sub-25nm patterns will be reviewed. A few proposed limiting factors of current etching tooling, underlying principles of different chemistries, and processing parameters and their advantage and drawback to etching nanometer scale features will also be discussed.