Abstract Submitted
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Ion heating rates in scalable trap architectures for quantum computation[1] R.J. EPSTEIN, D. LEIBFRIED, J.J. BOLLINGER, S. SEIDELIN, J.H. WESENBERG, N. SHIGA, J.M. AMINI, R.B. BLAKESTAD, J. BRITTON, K.R. BROWN, J.P. HOME, W.M. ITANO, J.D. JOST, E. KNILL, C. LANGER[2], R. OZERI[3], D.J. WINELAND, Time and Frequency Division, NIST, Boulder, CO 80305, USA — We describe the characterization of several microfabricated ion trap architectures for quantum computation. Our apparatus for testing planar ion trap chips[4,5] features: a standardized chip carrier for ease of interchanging traps, a single-laser Raman sideband-cooling scheme, and photo-ionization loading of Mg^+ ions. We measure the heating rate of an ion's motional degree-of-freedom, a factor which limits multi-ion logic gate fidelities. Two measurement techniques are compared, the standard Raman sideband technique and time-resolved fluorescence detection during Doppler re-cooling[4]. One of the traps, fabricated from gold on fused silica, shows heating rates below 1 quanta/ms (motional frequency = 5.3 MHz), boding well for planar ion trap designs.

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[4]S. Seidelin *et al.*, Phys. Rev. Lett. **96**, 253003 (2006).
[5]J. Kim *et al.*, Quantum Inf. Comput. **5**, 515 (2005).

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