Abstract Submitted
for the DAMOP10 Meeting of
The American Physical Society

Silicon surface-electrode ion traps for quantum information processing[1] S. CHARLES DORET, RICHART SLUSHER, Georgia Tech Research Institute — The Georgia Tech Research Institute (GTRI) is designing, building, and testing scalable surface-electrode ion traps for quantum information applications, fabricated using silicon VLSI technology. A wide range of trap architectures have been developed, including a linear trap capable of holding long chains of equally spaced ions, a 90-degree X-junction, and an integrated micromirror with collection efficiency approaching 20%. Fabrication features that can be integrated with the surface electrodes include multilayer interconnects, optics for enhanced light collection, flexible optical access through beveled slots extending through the substrate, and recessed wire bonds for clear laser access across the trap surface. Traps are designed at GTRI using in-house codes that calculate trap fields, compute the full motion of ions confined in the trap, including micromotion, and optimize electrode shapes and transport waveforms using genetic algorithms. We will present designs and initial test results for several of these traps, as well as plans for their use in future experiments.

[1]Support for this work provided by IARPA through the Army Research Office award W911NF081-0315 and by DARPA through award W911NF-07-1-0576.

S. Charles Doret
Georgia Tech Research Institute

Date submitted: 27 Jan 2010 Electronic form version 1.4