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Towards Quantum Simulations Using a Chip Ion Trap[1]
CHENGLIN CAO, KEN WRIGHT, DANIEL BRENNAN, GEOFFREY JI, CHRISTOPHER MONROE, Joint Quantum Institute, Department of Physics and National Institute of Standards and Technology, Univ of Maryland College Park, Maryland 20742 — We report our current experimental progress towards using chip ion traps for quantum simulation. Current progress is being made using a microfabricated symmetric trap from GTRI. This trap implements a novel two level design that combines the benefits of both surface traps and linear four-rod traps. The trap has 50 electrodes which allow for the fine control of the DC potential needed to create large anharmonic potentials, to join and split ion chains and to shuttle ions along the trapping axis similar to many surface traps. However this trap also has a much deeper trapping depth than conventional surface traps and improved optical access via an angled slot through the chip wide enough to accommodate higher power laser light which could cause surface charging or damage in a traditional chip trap. These advantages should allow trapping of long ion chains. We hope to use these features as the next step in increasing the size of current quantum simulations being done at Univ of Maryland, which are aimed at exploring quantum phenomena in spin systems in a regime inaccessible to classical simulation. This work is supported by grants from the U.S. Army Research Office with funding from the DARPA OLE program, IARPA, and the MURI program; and the NSF Physics Frontier Center at JQI.

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