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Exploiting Symmetry for Quantum Error Suppression YUNSEONG NAM, REINHOLD BLÜMEL, Wesleyan Univ — In light of recent experimental progress in quantum computing, the time is ripe to discuss quantum computer hardware optimization. Taking the digital/analog hybrid nature of quantum computers into account, choosing a proper processor architecture for a given quantum algorithm becomes crucial in making quantum computing a practical reality. As a first step in this direction, we investigate the robustness of quantum adders with respect to naturally occurring hardware defects and errors. In particular, we compare the robustness of the ripple-carry adder to that of the quantum Fourier adder. We show that, surprisingly, when used in Shor's algorithm, the quantum Fourier adder may well be more robust than the ripple-carry adder. We present a noise suppression scheme, called symmetric noise, applicable to the quantum Fourier architecture, that, measured in terms of fidelity, results in an order-of-magnitude performance boost.

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