

Abstract Submitted
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Bit-Error Ratio Testing of Xilinx FPGAs Using Pseudo-Random Binary Sequences ANDY GOERS, Iowa State University — With RHIC collision rates reaching orders of a MHz in pp reactions, it is vital that detector electronics are able to process the massive influx of data received every second. Much of this data processing is done by field programmable gate arrays (FPGAs). However, with any experimental setup, one must know the limitations of the apparatus. High speed electronics often see bit errors due to attenuation or simply from hardware failures. Bit errors in detector electronics can show up as bad data and even “fake” particles, so it is important to know how often these bit errors occur. Pseudo-random binary sequences (PRBS) are often used to test high speed electronics’ bit-error ratios (BER), or errant bits per bits received. A PRBS is generated using polynomials creating a seemingly random sequence of binary numbers. A BER can be measured by sending out and receiving a known PRBS and checking for errors in the received sequence. I will present results of BER testing of gigabit transceiver protocols on Xilinx Virtex 5 LXT50T and LXT110T FPGAs for PHENIX detector electronics upgrades.

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