Abstract Submitted
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12-bit 32 channel 500MS/s low-latency ADC for particle accelerators real-time control.[1] ANTON KARNITSKI, DALIUS BARANAUSKAS, DENIS ZELENIN, GYTIS BARANAUSKAS, ALEXANDER ZHANKEVICH, CHRIS GILL, None — Particle beam control systems require real-time low latency digital feedback with high linearity and dynamic range. Densely packed electronic systems employ high performance multichannel digitizers causing excessive heat dissipation. Therefore, low power dissipation is another critical requirement for these digitizers. A described 12-bit 500MS/s ADC employs a sub-ranging architecture based on a merged sample & hold circuit, a residue C-DAC and a shared 6-bit flash core ADC. The core ADC provides a sequential coarse and fine digitization featuring a latency of two clock cycles. The ADC is implemented in a 28nm CMOS process and consumes 4mW of power per channel from a 0.9V supply (interfacing and peripheral circuits are excluded). Reduced power consumption and small on-chip area permits the implementation of 32 ADC channels on a 10.7mm^2 chip. The ADC includes a JESD204B standard compliant output data interface operated at the 7.5Gbps/ch rate. To minimize the data interface related time latency, a special feature permitting to bypass the JESD204B interface is built in.

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