DPP11-2011-020024

Abstract for an Invited Paper
for the DPP11 Meeting of
the American Physical Society

Plasma Etching - The Challenges Ahead in Enabling Nanoelectronics

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Plasma etching has enabled the perpetuation of Moore's Law from >1 μm to now less than 20 nm. More than ever, plasma etching is used to enable the extension of semiconductor device fabrication into the nanoelectronics age. Etching is used to compensate for lithographic limitations in resolution and line width roughness; more recently, etching is used to compensate for non-uniformities in up-stream deposition processes. Yet, plasma etching has also pushed against fundamental limitations for many years: e.g., aspect ratio and more generally pattern dependent etching, atomic-scale mixing, and wafer-edge discontinuities. In this talk, I will review the origins of these limitations and what options are available going forward to circumvent them. Pulsed plasma technology, whereby a temporal separation of ion and neutral flux to the wafer is crudely achieved, has proved beneficial for reducing charging effects that contribute to aspect ratio dependent etching. Pulsing also enables tuning plasma etch processes from a neutral-limited regime to an ion-limited regime and thereby enables a more effective usage of the anisotropic transport of ions into nano-structures. Selectivity is arguably an even larger challenge as requirements for fabrication of the most advanced logic devices demand atomic layer etching. Is this feasible? Modulated plasma processing has shown some process in improving stop-layer selectivity, but how far can this method be applied? Finally, I will review the long-standing issues with finite wafer size and how the industry has coped to date with the trade-offs imposed by discontinuities on the wafer edge.