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Design Considerations in Capacitively Coupled Plasmas SANG-HEON SONG, TEL Technology Center, PETER VENTZEK, Tokyo Electron America, ALOK RANJAN, TEL Technology Center — Microelectronics industry has driven transistor feature size scaling from 10^{-6} m to 10^{-9} m during the past 50 years, which is often referred to as Moore's law. It cannot be overstated that today's information technology would not have been so successful without plasma material processing. One of the major plasma sources for the microelectronics fabrication is capacitively coupled plasmas (CCPs). The CCP reactor has been intensively studied and developed for the deposition and etching of different films on the silicon wafer. As the feature size gets to around 10 nm, the requirement for the process uniformity is less than 1-2 nm across the wafer (300 mm). In order to achieve the desired uniformity, the hardware design should be as precise as possible before the fine tuning of process condition is applied to make it even better. In doing this procedure, the computer simulation can save a significant amount of resources such as time and money which are critical in the semiconductor business. In this presentation, we compare plasma properties using a 2-dimensional plasma hydrodynamics model for different kinds of design factors that can affect the plasma uniformity. The parameters studied in this presentation include chamber accessing port, pumping port, focus ring around wafer substrate, and the geometry of electrodes of CCP.

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