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Porous Low-k Material Etch For 32 nm and Beyond YIFENG ZHOU, QINGJUN ZHOU, RYAN PATZ, HAIRONG TANG, JEREMIAH PENDER, MICHAEL ARMACOST, Applied Materials, Inc., CATHERINE LABELLE, Advanced Micro Devices, DAVID HORAK, IBM Research, APPLIED MATERIALS, INC. TEAM, ADVANCED MICRO DEVICES TEAM, IBM RESEARCH TEAM — Porous low-k materials with k ∼2.2 pose new challenges for plasma etch/strip damage, rough etch front/micro-trenching and via faceting are the top issues in ULK all-in-one etch. In this paper, low-k damage has been characterized for both etch and strip. The impacts of etch and strip on ULK etch and dependence of via faceting on plasma conditions and plug height have been studied. Process window of faceting control has also been discussed. It has been demonstrated that all-in-one etch and strip for via first approach can be extended to ULK (2.2) integration.

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