

Abstract for an Invited Paper  
for the GEC10 Meeting of  
The American Physical Society

### **Plasma Processing for Nanoelectronics — History and Prospects<sup>1</sup>**

MICHAEL LIEBERMAN, UC Berkeley

Plasma processing is a crucial technology for fabricating trillions of nanometer-size transistors on a silicon wafer [1]. It evolved from humble beginnings in the early 1900's: the silver-coating of mirrors by physical sputtering in dc glow discharges. The late 1950's - early 1960's saw extensive studies of physical and reactive sputtering in capacitive rf reactors. Isotropic plasma etching, mainly for photoresist stripping, was developed in the late 1960's - early 1970's, and etching of many other important materials was demonstrated. Three key advances in the late 1970's made plasma processing technology indispensable: (a) the discovery of ion-enhanced (anisotropic) etching [2]; (b) the development of SiO<sub>2</sub> etching with high SiO<sub>2</sub>/Si selectivity [3]; and (c) the controlled etching of passivating films, eg, Al<sub>2</sub>O<sub>3</sub> over Al [4]. As scale-down to current 32 nm (100 atom) transistor gate lengths proceeded, etching discharges evolved from a first generation of "low density" reactors capacitively driven by a single source, to a second generation of "high density" reactors (inductive and electron cyclotron resonance) having two power sources, in order to control independently the ion flux and ion bombarding energy to the substrate. A third generation of "moderate density" reactors, driven capacitively by multiple frequency sources, is now used to further control processing characteristics, such as ion energy distributions, uniformity, and selectivity. There is yet much to be understood, e.g., the physics of multiple-frequency sheaths, nonlinear frequency interactions, and electromagnetic effects such as standing waves. Beyond the 6–11 nm transistor limit lies a decade of further improvements for conventional nanoelectronics, and beyond that, a dimly-seen future of spintronics, single-electron transistors, cross-bar latches, and molecular electronics.

[1] H. Abe, M. Yoneda and N. Fujiwara, "Developments of Plasma Etching Technology for Fabricating Semiconductor Devices," Jpn. J. Appl. Phys. 47, 1435 (2008).

[2] N. Hosokawa, R. Matsuzaki and T. Asamaki, "RF Sputter-Etching by Fluoro-Chloro-Hydrocarbon Gases," Jpn. J. Appl. Phys. Suppl. 2, Pt. 1, 435 (1974).

[3] R.A.H. Heinecke, "Control of Relative Etch Rates of SiO<sub>2</sub> and Si in Plasma Etching," Solid State Electronics 18, 1146 (1975).

[4] S.I.J. Ingrey, H.J. Nentwich, and R.G. Poulsen, "Gaseous Plasma Etching of Al and Al<sub>2</sub>O<sub>3</sub>," USP 4,030,967 (filed 1976).

<sup>1</sup>Supported by UC Discovery Grant ele07-10283 under the IMPACT program and the Department of Energy Office of Fusion Energy Science Contract DE-SC0001939; special thanks to J.W. Coburn