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Challenges in the Plasma Etch Process Development in the sub-20nm Technology Nodes

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For multiple generations of semiconductor technologies, RF plasmas have provided a reliable platform for critical and non-critical patterning applications. The electron temperature of processes in a RF plasma is typically several electron volts. A substantial portion of the electron population is within the energy range accessible for different types of electron collision processes, such as electron collision dissociation and dissociative electron attachment. When these electron processes occur within a small distance above the wafer, the neutral species, radicals and excited molecules, generated from these processes take part in etching reactions impacting selectivity, ARDE and micro-loading. The introduction of finFET devices at 22nm technology node at Intel marks the transition of planar devices to 3-dimensional devices, which add to the challenges to etch process in fabricating such devices. In the sub-32nm technology node, Back-end-of-the-line made a change with the implementation of Trench First Metal Hard Mask (TFMHM) integration scheme, which has hence gained traction and become the preferred integration of low-k materials for BEOL. This integration scheme also enables Self-Aligned Via (SAV) patterning which prevents via CD growth and confines via by line trenches to better control via to line spacing. In addition to this, lack of scaling of 193nm Lithography and non-availability of EUV based lithography beyond concept, has placed focus on novel multiple patterning schemes. This added complexity has resulted in multiple etch schemes to enable technology scaling below 80nm Pitches, as shown by the memory manufacturers. Double-Patterning and Quad-Patterning have become increasingly used techniques to achieve 64nm, 56nm and 45nm Pitch technologies in Back-end-of-the-line. Challenges associated in the plasma etching of these multiple integration schemes will be discussed in the presentation.

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