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Modeling of plasma-induced damage during the etching of ultimately-scaled transistors in ULSI circuits—A model prediction of damage in three dimensional structures[1]

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An increasing demand for high performance field-effect transistors (FETs) leads to the aggressive critical dimension shrinkage and the currently-emerging three dimensional (3D) geometry [1]. Plasma processing is widely used also in the scaled- and 3D-FET (e.g. FinFET) manufacturing, where precise control of the reaction on the (sidewall) surfaces is a prime issue. In this study, damage creation mechanism during plasma etching—plasma-induced physical damage (PPD)—was investigated in such structures on the basis of the PPD range theory [2], atomistic simulations, and experiments. Compared to PPD in planar FETs (e.g. Si recess [2][3]), a stochastic modeling and atomistic simulations predicted that, during etching of "fins" in a 3D-FET, the following two mechanisms are responsible for damage creation in addition to an ion impact on the sidewall at an oblique incident angle: 1) incoming ions penetrate into the Si substrate and undergo scattering by Si atoms in the lateral direction even if the incident angle is normal to the surface [4] and 2) some of Si atoms and ions sputtered at the surface being etched impact on the sidewall with energies sufficient to break Si-Si bonds. These straggling and sputtering processes are stochastic and fundamental, thus, result in 3D structure damage ("fin-damage"). The "fin-damage" induced by straggling was modeled by the PPD range theory. Molecular dynamics simulations clarified the mechanisms under the various plasma conditions. Quantum mechanical calculations showed that created defect structures play the role of a carrier trap site, which was experimentally verified by an electrical measurement. Since they are intrinsic natures of etching, both straggling and sputtering noted here should be implemented to design a low-damage etching process.

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