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Atomic Layer Etch: A Concurrent Plasma Modeling and Process Approach

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Atomic layer etching (ALE) has been investigated over decades and is getting more attention recently than ever due to its potential capability of solving grand challenges in advanced node plasma etch. As feature size shrank to nanometer scale, etch issues such as ARDE, loading, etch stop, top clogging etc. turned to be more severe than in more relaxed patterning schemes. However, ALE, as a promising solution to all problems in traditional etch methods, has its own challenges. Questions that are frequently asked regarding self-limiting process, productivity, hardware capability, etc. have to be considered during an ALE process development. To precisely control ALE processes, fundamental understanding of the surface interactions during etch is required. In this talk, we will discuss concurrent engineering approaches including both modeling and experiment to understand and develop ALE etching processes that meet grand challenge requirements. The core of the approach is an integrated chamber scale HPEM (Hybrid Plasma Equipment Model)-feature scale MCFPM (Monte Carlo Feature Profile Model) model [1]. The concurrent engineering approach comprises stages of development and prediction capability tests using both blanket wafer and patterned stack data and finally process parameter optimization. By using this approach, we are able to provide insights on how to resolve grand challenges in plasma etch with a minimum of engineering resources. The presentation will survey both experimental and computational results representing a few case studies in SAC quasi-ALE, Si ALE, Si3N4 ALE, etc. Furthermore, insights into the relationship between chamber function and critical surface interactions will be discussed. [1] M.Wang and M.Kushner, J. Appl. Phys 107, 2010.