

MAR05-2004-000522

Abstract for an Invited Paper  
for the MAR05 Meeting of  
the American Physical Society

### **Physics of Modern VLSI CMOS**

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The Integrated Circuit (IC) was invented in 1958, and modern CMOS was invented in 1980. The semiconductor physics that underlies the IC was discovered in the early part of the past century, and, by the early 60's, it was simplified and codified such that it could be used by engineers to design transistors of ever shrinking size and increasing performance. However, in the past 5-10 years, the "engineering physics" of the 60's is becoming increasingly inadequate. Empirical corrections are being made to allow for quantum and non-equilibrium Boltzmann transport effects. Moreover, as features in CMOS transistors reach atomic dimensions, continuum physics is no longer adequate, and devices must be designed increasingly, at the atomic level. In the past 30 years, transistor gate length has shrunk by a factor of 100X: from 10  $\mu\text{m}$  to 0.1  $\mu\text{m}$ . And it is expected to shrink by about another factor of 10X to 10 nm in the next 10-15 years. However, as transistors approach the end of scaling, the physics to design them will become increasingly complex:

- Gate oxide, which is today a few monolayers (10A) thick will be replaced with new materials with high dielectric constant.
- Metal gate electrodes will replace poly-Si, and the interface, which sets the effective work-function, needs to be understood.
- Carrier scattering in the inversion layer in the presence of increasingly high electric fields (horizontal and vertical) needs to be better understood.
- Tunneling will increasingly dominate transistor behavior.
- The discrete positioning of dopants will increasingly affect transistor performance.
- Transistors will become increasingly ballistic.
- Stress in the channel is increasing to the point where it has large impact on device performance.
- And new materials will be introduced into the Source/Drain and channel.

Each of these issues will be discussed, and the unresolved physics issues will be identified