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Metal screening for CMOS application through vacuum and interface work function ab-initio calculations: benefits and limitations

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Future reduction of transistor dimensions in line with historical trends cannot be achieved with the current SiO_2/polysilicon technology due to limited effective oxide thickness (EOT) scalability and excessive power consumption caused by high gate leakage current. Among the proposed solutions, the high permissivity dielectric (high-K)/metal combination seems to be a promising route. While considerable progress has been made towards identifying a favorable high-K dielectric, with HfO_2 and its silicates and nitrides as the leading candidates, n- and p-type metal gates with appropriate work functions still lack. A rough, "first order" metal gate screening can be performed with considerable confidence through measurement and calculation of metal vacuum work functions (WFs). However, charge exchange at metal/dielectric interfaces cause the metal effective WF on a particular dielectric to differ from its vacuum value, sometimes by as much as 1 eV [1]. For that reason, metal effective WF *ab-initio* calculations using interface models are of primary importance if theory is to be used as a guide for correctly identifying metal gates. In this talk I will discuss the role of interface states on the pinning of metal Fermi levels and show results for model HfO_2/Si and Al_2O_3/Si interfaces that correctly reproduce experimental data with polysilicon as the gate metal [2]. Next I will describe results of theoretical metal screening for polysilicon replacement. We have found that while vacuum WF calculations can be quite accurate, hence useful as a predictive tool, metal/dielectric interface calculations are severely limited in accuracy by the lack of experimental information on the atomistic structure of the interfaces and possibly by an unexpected and still unclear drawback of density functional theory (DFT) within the local density approximation (LDA) [3]. Improvements based on empirical scaling of the DFT/LDA calculated metal/dielectric valence band offset and on bulk GW calculations of the dielectric valence band edge shift with respect to DFT/LDA results will be discussed. Finally I will describe experimental difficulties encountered when trying to modulate metal WFs through interface engineering and how simulations have contributed to understand why that may be so.
[1] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, Appl. Phys. Lett. **85**, 1826 (2004). [2] C.C. Hobbs *et al.*, *IEEE Trans. Elec. Dev.* **51**, 971/978 (2004). [3] L. R. C. Fonseca and A. A. Knizhnik, unpublished.