

Abstract Submitted
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Layered Tunnel Barrier Lowering in High-k Heterostructures using Bias-dependent Internal Photoemission Spectroscopy DOUGLAS BELL, Jet Propulsion Laboratory, JULIE BREWER¹, Caltech, HARRY ATWATER, Caltech — Layered tunnel barriers have been proposed as replacements for SiO₂ for use as injection barriers in nanocrystal floating-gate memories. Due to the predicted larger change in conductance as a function of injection voltage, such barriers are expected to enable nanosecond programming and erase times with archival data retention times. We have utilized internal photoemission (IPE) spectroscopy to study barrier height lowering of Al₂O₃/HfO₂/SiO₂/Si layered tunnel barrier structures over a wide range of applied biases. 15 nm layers of Al₂O₃ and HfO₂ were grown on n-Si substrates by atomic layer deposition. The IPE results are analyzed using a simple electrostatic model to yield effective barrier heights and overall band alignments across the entire voltage range. Using this technique we demonstrate substantial barrier lowering (~ 0.75 eV) for Si-compatible dielectric heterostructures, and we discuss the application of these barriers to improved speed and reliability of floating gate nonvolatile memory devices.

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