MAR05-2004-001169

Abstract for an Invited Paper
for the MAR05 Meeting of
the American Physical Society

High Performance Schottky Barrier MOSFETs

HORNG-CHIH LIN, Department of Electronics Engineering, National Chiao Tung University

Schottky barrier metal-oxide-semiconductor field-effect transistor (SB MOSFETs) has been recognized as one of the potential candidates for nano-scale device applications. Nevertheless, the inherent high off-state leakage and poor on/off current ratio represent major showstoppers for nano-scale device operation. We have recently reported the fabrication of a novel SB SOI MOS transistor featuring electrical source/drain junctions induced by a sub-gate overlying the passivation oxide. Pt or Co salicide process was adopted to form the Schottky barrier source/drain (S/D). The new device is extremely simple in fabrication and requires no implantation or associated annealing steps. We have shown that, a proper sub-gate bias could not only increase the on-state current but also significantly suppress the off-state current. In addition, the device is capable of bi-channel operation, which is unique, interesting, and greatly simplifies CMOS process integration. Ambipolar device characteristics with excellent on/off current ratios ($>10^8$) have been demonstrated on a same single device with $CoSi_2$ S/D. Moreover, near-ideal sub-threshold swing ($\sim$ 60 mV/decade) for both n- and p-channel modes of operation could be realized on a same single device, as the planar channel length is scaled to less than 100 nm.