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Surface Roughness and Dislocation Distribution in Compositionally Graded Relaxed SiGe Buffer Layer with Inserted Strained Si Layers TAE-SIK YOON, JIAN LIU, YA-HONG XIE, Department of Materials Science and Engineering, University of California Los Angeles — We report the experimental investigation of surface roughness and dislocation distribution of 1 μ m-thick, compositionally graded, relaxed SiGe buffer layer with a final Ge surface content of 30%. Tensile-strained Si layers are inserted at various locations in the graded buffer during SiGe epitaxial growths. Slight reduction in surface roughness from about 10.3 nm to about 7.8 nm by inserting two 20 nm thick tensile-strained Si layers followed by SiGe growths. It turns out that majority of the residual surface roughness is developed during the SiGe growths on top of the topmost strain Si layer. The surface immediately after the growth of tensile strained Si is very flat with about 1.1 nm RMS roughness and without crosshatch morphology. Cross-sectional TEM shows clear signs of increased interaction between dislocation half-loops at the top surface of the strained Si layers. Our observation shows that although thin Si layers under tensile-strain are effective in reducing cross-hatch, they could in the meantime impede dislocation propagation leading to higher threading dislocation density. Considerations for an optimized scheme exploiting the flattening function of tensile-strained layers will be discussed.

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