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Imaging of "fully depleted" ultra-thin silicon-on-insulator by scanning tunneling microscopy PENGPENG ZHANG, EMMA TEVAARWERK, MARK ERIKSSON, DONALD SAVAGE, MAX LAGALLY — Silicon-on-insulator has emerged as an important substrate in MOSFET technology. Silicon template layers with normal doping level of 10^{15}cm^{-3} and as thin as 10nm will be depleted of free carriers by interface states at the Si-SiO_2 or Si-vacuum (when the silicon template is clean) interfaces [1]. As suggested by previous studies [2, 3], it should therefore be impossible to perform scanning tunneling microscopy (STM) measurements on very thin SOI surfaces. We show such considerations to be incorrect: we present high-quality STM images on "fully depleted" 10nm SOI(001) and 15nm strained Si-on-insulator [sSOI(001)], as well as Ge-covered SOI(001). We believe that surface π and π^* bands are responsible for the ability to conduct even though there are no free "bulk" charges. Carriers can be easily thermally excited across the reduced surface bandgap (0.5-0.6eV). We discuss prior results in light of our findings, as well as the potential effect of surface states on conduction as the Si template layer becomes thinner and thinner. Research supported by DOE and AFOSR [1] S. Henaux, et al. J. Electrochem. Soc. 146, 2737 (1999) [2] K. C. Lin, et al. Appl. Phys. Lett. 72, 2313 (1998) [3] P. Sutter, et al. Appl. Phys. Lett. 85, 3148 (2004)

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