Abstract Submitted
for the MAR05 Meeting of
The American Physical Society

**Nanopatterned circuits in silicon: towards gain and logic** BONNIE A. SHERIFF, J.E. GREEN, E. JOHNSTON-HALPERIN, R.A. BECKMAN, J.R. HEATH, Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, CA — High density arrays of doped silicon nanowires (NWs) have been demonstrated using the SNAP technique. This technology enables the fabrication of nanoscale memory devices, field effect transistor (FET) arrays, and biological and chemical sensors. Here we report the development of a laterally patterned diffusion doping technique which utilizes a batch compatible spin-on glass process to achieve spatial control of both p- and n-type dopants. This enhanced control allows for the fabrication of nanoelectronic gain elements, such as p-n diodes, and n-p-n and p-n-p transistors, as well as circuits that combine n-FET and p-FET arrays into mosaics capable of CMOS-compatible logic. Here, we use electrostatic force microscopy (EFM) to verify the fidelity of the patterned doping process and characterize active devices, while current-voltage measurements evaluate junction quality and device performance.

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Date submitted: 30 Nov 2004 Electronic form version 1.4