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High Speed Spin-Transfer Switching Behavior of Low Critical Current Spin Valve Nanopillars P.M. BRAGANCA, I.N. KRIVOROTOV, O. OZATAY, A.G.F. GARCIA, J.C. SANKEY, N.C. EMLEY, D.C. RALPH, R.A. BUHRMAN, Cornell University — For spin transfer writing to be effective for MRAM, the integration of a magnetic device with a scaled CMOS transistor in a memory cell requires that I_c for switching a thin, thermally stable element on ns time scales be $<<$ 1 mA. Since I_c scales with the volume of the magnetic element and the square of its saturation magnetization M_S, the use of very small free layers with low M_S can result in low I_c's. The challenge is obtaining a large enough magnetic anisotropy to ensure thermal stability at $\sim$100 C. We have fabricated 40x120 nm elliptical Py/Cu/Py nanopillar spin valves exhibiting free layer coercive fields in accord with 3-D micromagnetic modeling. For a 4.5 nm thick free layer device, currents necessary for 100% switching go from 0.6 mA for a 10 ns pulse, where thermal activation aids switching, to 2 mA for a 1 ns pulse, where there is insufficient time for thermal fluctuations and I_c is set by the current required to transfer enough spin into the free layer to force its reversal. We will discuss the switching mechanisms of these devices in the ns regime, and our progress towards achieving fully stable devices with low I_c's.

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