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Atomic-scale challenges in nano-MOSFETs: Gate dielectrics and device modeling[1]

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As microelectronics enters the regime of nano-scale dimensions, new materials are being introduced and new challenges emerge in modeling devices, as standard approximations break down. The channel and gate dielectric in MOSFETS present key challenges as normal Si is replaced by strained Si in the channel, Silicon-on-Insulator technology leads to the adoption of double gates, and SiO_2 is replaced by "alternate dielectrics." The talk will address issues on interface structure and electronic properties of alternate dielectrics and present new results obtained by first-principles and atomic-resolution Z-contrast microscopy; address reliability issues such as negative bias temperature instability; describe mobility calculations by first-principles theory and atomic-scale interface models, and describe first-principles calculations of Fowler-Nordheim tunneling.

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