Abstract Submitted for the MAR05 Meeting of The American Physical Society

Surface passivation and high-k dielectrics in Si nano-FETs JONATHAN E. GREEN, E. JOHNSTON-HALPERIN, K. BEVERLY, R.A. BECK-MAN, B.A. SHERIFF, Y. LUO, J.R. HEATH, Department of Chemistry, Caltech, Pasadena, CA — Scaling limitations in contemporary ULSI/VLSI technology have sparked an intense effort to seek alternatives to conventional CMOS-based computing. While much of this effort has consisted of attempts to reduce device size, a more appropriate figure of merit for a scalable architecture is device density. Accordingly, issues such as device pitch and power consumption are also relevant. We have previously demonstrated that SNAP nanowire arrays can simultaneously address both device size (down to 10 nm by 100 nm) and density (pitch down to 35 nm) through the generation of arrays of Si nanowire FETs. However, the concurrent issue of power consumption remains a significant technical problem. One route to increased efficiency is the use of high-k dielectrics (such as HfO_2) and careful control of the nanowire-dielectric interface. To that end, we explore the impact of various surface passivation schemes, dielectrics, and crystal orientations on SNAP-based nano-FET performance.

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Date submitted: 01 Dec 2004

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