Defects at Si-SiO$_2$ and internal dielectric interfaces in high-k gate stacks for Si devices

GERALD LUCOVSKY, Dept. of Physics, North Carolina State Univ., Raleigh, NC, J.C. PHILLIPS, Rutgers University — The performance and reliability of Si field effect transistors (FETs) are determined in large part by electronically-active defects/defect precursors at the Si-SiO$_2$, and internal SiO$_2$-high-k dielectric interfaces. Defect/defect precursor reduction is associated with bond-strain driven interfacial self-organizations taking place during high temperature, inert ambient annealing and are addressed through the application of bond constraint theory to the Si-SiO$_2$, and internal SiO$_2$-high-k dielectric interfaces. The Si-SiO$_2$ interface is crucial with respect to interface trapping, and scattering of charge carriers in the FET channels. An empirical roughness scattering parameter at this interface reflects the scale of the interfacial self-organization, $\sim 5$ nm. The step in the average number of bonds/atom at the internal dielectric interface determines the fixed charge density, $Q_f$, at that interface, and has been reduced by more than a factor of ten by self-organizations in devices with Hf and Zr high-k dielectrics.

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