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Enhanced permittivity of the interfacial oxide in gate insulator stacks on silicon ALFREDO PASQUARELLO, FELICIANO GIUSTINO, EPFL Lausanne (Switzerland) — While transition metal oxides are currently under consideration for the scaling of the equivalent oxide thickness in MOS devices, a thin SiO₂ layer often forms at the channel interface during the deposition process, affecting the gate capacitance. Within a density functional approach, we investigate the dielectric permittivity and estimate the equivalent oxide thickness of this interfacial layer. For this purpose, we consider a realistic model of the Si-SiO₂ interface which takes into account the amorphous nature of the oxide. Our calculations indicate that the static permittivity of the 0.5 nm thick interfacial layer is about 50% larger than that of bulk silica. As a consequence, the equivalent thickness of the substoichiometric layer is smaller than the corresponding physical thickness by 0.2–0.3 nm. By spatially mapping the frequency-dependent dielectric response, we show that the enhanced permittivity of the interfacial layer originates from the larger electronic contribution of the Si–Si bonds and from the softening of the infrared active modes in the substoichiometric oxide.

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