Abstract Submitted for the MAR05 Meeting of The American Physical Society

Silicon nanoscale 2D donor devices fabricated by UHV-STM lithography J.S. KLINE, S.J. ROBINSON, J.R. TUCKER, University of Illinois at Urbana-Champaign, T.-C. SHEN, Utah State University, C. YANG, R.-R. DU, University of Utah, Y. LIU, X. WANG, T.P. MA, Yale University — We developed a scheme to fabricate nanoscale electronic devices by patterning 2D shallow donors into single crystal silicon. The goal of this approach is to seamlessly integrate nanoand microelectronics. In this approach, we pattern the devices on H terminated Si(100)-2x1 surfaces via UHV-STM. Phosphine molecules selectively adsorb onto the patterned areas to define conduction pathways. Low temperature Si MBE is used to encapsulate the dopants in the Si lattice. Two-terminal electrical connection to the outside-world is provided by a template structure formed by conventional microfabrication. A third terminal used for gate modulation of the device is formed by silicon nitride jet vapor deposition and metallization. Low temperature electrical characterization of conducting wires show significant departure from Ohmic conduction for width < 50 nm. Electro and magnetotransport properties will be discussed. Tunnel junction and single electron transistor fabrication are currently underway. The low charged-defect density provided by complete encapsulation could allow the fabrication of a solid state quantum computer.

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Date submitted: 01 Dec 2004

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