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Molecular beam epitaxy for advanced gate stack materials and processes

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The material requirements for future CMOS generations - as given by the ITRS roadmap - are very challenging. This includes a high K dielectric without a low K interfacial layer, a high mobility channel and the appropriate metal gate. With the help of two projects INVEST and ET4US, we are building up a molecular beam epitaxy (MBE) infrastructure to grow this material set on large area wafers that can be further processed into small scale devices. In the INVEST project, we have developed an MBE system for the growth of complex oxides on semiconductors. The system follows the overall design of a production tool and is equipped with an RF atomic oxygen source, effusion cells, e-beam evaporators and a differential pumping stage. The oxide growth process starts with desorbing the initial surface oxide on the Si wafers in ultra-high vacuum and high temperature to create a clean reconstructed 2×1 surface. Using the atomic oxygen it is possible to oxidize the surface in a well controlled manner at low temperature and to grow very thin and dense SiO_x layers, followed by the growth of 2-6 nm amorphous high K dielectrics. The process parameters permit to tune the interface layer from a SiO_x rich to a silicide rich interface with a significant impact on the capacitance and the leakage. Initial focus is on developing an optimized growth recipe for high quality amorphous HfO_2 and $\text{LaHfO}_{3.5}$ films. This recipe was subsequently used to make wafers for a transistor batch that gave us the first N short channel MBE MOSFET's (100 nm) using an etched gate process flow. Some highlights of the first batch for 3nm HfO_2 MOSFET are a high mobility ($> 270 \text{ cm}^2/\text{Vs}$) with a corresponding low leakage current of $2 \text{ mA}/\text{cm}^2$). While there were some process issues for $\text{LaHfO}_{3.5}$, the 3 nm MOSFET showed very low leakage currents below $10^{-6} \text{ A}/\text{cm}^2$. Interestingly all the $\text{LaHfO}_{3.5}$ MOSFETs showed very low threshold voltage instabilities. In collaboration with C. Marchiori, M. Sousa, A. Guiller, H. Siegwart, D. Caimi, J. Fompeyrine, D. J Webb, C. Rossel, R. Germann of IBM Research GmbH Zurich Switzerland; L. Pantisano, M. Claes, T. Conard, M. Demand, W. Deweerdt, S. DeGendt, M. Heyns, M. Houssa, M. Aoulaiche, G. Lujan, L. Ragnarsson, E. Rohr, T. Schram of IMEC Leuven Belgium; J. Hooker, Z.M Rittersma, Y. Furukawa of Philips Research Leuven Belgium and J. W. Seo of EPFL Lausanne Switzerland.