

Abstract Submitted
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Nanowire and nanotube transistors with surrounding gates
ZHICHENG LUO, BO LEI, XIAOLEI LIU, CHAO LI, CHONGWU ZHOU, University of Southern California — We will present fabrication and electronic transport studies of novel nanowire and nanotube transistors with surrounding polymer-electrolyte gates. These devices are based on nanowires/nanotubes contacted by source/drain electrodes atop Si/SiO₂ substrate. Vias were etched through the SiO₂ layers, followed by refilling LiClO₄/poly(ethylene oxide). The silicon substrate is thus in electrical contact with the polymer electrolyte, therefore forming the surround gate for the transistors. Electronic characterization revealed well-enhanced transconductance for both nanowire and nanotube transistors, with operating gate voltage reduced to 1V. In addition, intriguing negative differential resistance has been observed with surround-gated nanowire transistors, which can be attributed to the much enhanced gate dependence.

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