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Straining Si on Insulator

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Transistor scaling has been the primary factor driving mainstream Si CMOS performance improvement. Approaching the fundamental limits of conventional bulk transistor scaling makes it increasingly difficult to remain on the historic scaling trend. To solve the two major scaling issues, namely increases in transistor leakage and decrease in performance improvement, new materials and device architectures are demanded. Two parallel developments in Si CMOS technology have created new opportunities in the control of channel electrostatics and the improvement of channel transport, for leakage reduction and performance enhancement. The two developments are: silicon-on-insulator (SOI) and strained channel. Due to excellent channel electrostatics, SOI transistors are considered very scalable, with their architecture scaling from partially depleted SOI for the current generation to fully depleted variety for future generations. Appropriately applied strain to the device channel can significantly increase channel mobility, and consequently increase drive current. Both technologies can be incorporated into the CMOS device structure to significantly improve its scalability and boost its performance. In this paper, we will first describe how these two advances allow further scaling of CMOS, which include scalability improvement in SOI devices and performance enhancement by channel strain engineering. Of particular interest is the strain engineering for SOI platforms, including strained substrates and process-induced strain, leading to SiGe-on-insulator (SGOI), strained-Si-on-insulator (SSOI), and other process-induced strain techniques based on SOI substrates. We will describe the formation of such engineered substrates, implementation of the strain-engineered processing, as well as their impact on MOSFET performance.