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High-resolution characterization of advanced interconnect and packaging architectures SHRIRAM RAMANATHAN, Components Research, Intel Corp., EVAN PICKETT, Intel, PATRICK MORROW, Intel, YONGMEI LIU, Intel, RAJEN DIAS, Intel — Characterization of buried interfaces in advanced interconnect and packaging structures is a critical challenge as CMOS devices are scaled and as novel packaging concepts such as through-silicon vias are developed. It is important to be able to image chip-to-package attach bumps with high resolution as well as individual interconnect layers in a processed device. Critical information that needs to be obtained from such inspection includes detection of un-bonded bumps, missing interconnections in stacked die and delaminations in underlying layers. In this paper, we discuss and benchmark different characterization techniques to analyze and quantify the quality of buried interfaces with detailed experimental and theoretical analyses. Acoustic microscopy is used to investigate interfaces between stacked die at high resolution. We present theoretical analysis which shows the effect of aberrations on image formation and the corresponding resolution degradation. Infra-red imaging through the substrate and pulsed thermal microscopy in transient mode were also used to investigate the quality of stacked die interfaces. We critically review these different techniques for inspection of buried interfaces and discuss roadmap for metrology needs.

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