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The Search for New Information Processing technologies¹

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Our society has benefited from the Golden Age of Electronics for the last half century. The ubiquitous transistor, in its many manifestations, has enabled an explosion of capabilities in information processing, communications, and sensing that has spurred exponential growth in performance-benefit ratios. Much of the credit for this progress is due to the continued scaling of the silicon integrated circuit (IC) components and to the associated efficient fabrication processes that have made the IC affordable. There is a growing realization, from simple physics arguments, that as minimum features sizes approach the ten nanometer regime, scaling will very likely slow and eventually end. This doesn't mean that the MOSFET will disappear, but more likely that it will need to be supplemented by other device and interconnect technologies if the exponential gains are to continue. In this talk we discuss the basis for the projected limitation of scaling of charge-based devices for logic and memory devices. We argue that a fundamental consideration for all devices, including those based on charge, relates to the capacity to manage heat generated by circuit operation. Our preference is for devices that operate at room temperature since the energy costs for cooling the devices must also be charged against the overall system energy consumption. (Cooling costs increase as a power of the difference between the ambient and the target temperature.) Therefore we seek new state variables to serve as an alternative to electrical charge for future information processing technologies. These technologies must provide the potential for sustaining exponential performance-cost benefits with time. The search must not only focus on device structures but on the underlying materials and process technologies that enable these structures. Indeed, to obtain extremely scaled CMOS, new materials and processes must also be developed. In this talk, we survey some of the candidates for replacements/supplements for/to the MOSFET and give a status report on the status of the search. We also briefly discuss the problem of design in the far nanometer regime where device variability is likely to be significant. What design constraints must be employed to ensure that manufacturing yields are high, given broad tolerance margins for the device characteristics? Variability is a growing problem in extremely scaled CMOS what is learned from these applications will likely benefit replacement technologies as well.

¹In Collaboration with Victor Zhirnov