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Scanning Probe Microscopy for Atomic-scale Silicon Device Fabrication

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Over the past three decades the driving force behind the expansion of the microelectronics industry has been the ability to pack ever more features onto a silicon chip, achieved by continually miniaturising the size of the individual components. However, after 2015 there is no known technological route to reduce device sizes below 10nm. In this talk we demonstrate a complete fabrication strategy towards atomic-scale device fabrication in silicon using a combination of scanning tunneling microscopy and high purity crystal growth. In particular we overcome one of the major obstacles to making functional semiconductor devices with an STM – connecting macroscopic leads to the device once it is removed from the vacuum environment [1]. We demonstrate key steps of the fabrication process, including the ability to place individual phosphorus atoms in silicon at precise locations [2] and encapsulate them in epitaxial silicon with minimal diffusion and segregation of the dopants [3]. We present magnetoresistance data showing the cross-over from 2D to 1D transport in nano-scale quantum wires and arrays. Finally we discuss the implications of these results for the construction of more sophisticated atomic-scale devices in silicon such as a silicon based quantum computer. [1] F.J. Ruess, L. Oberbeck, M.Y. Simmons, K.E.J. Goh, A.R. Hamilton, T. Hallam, N.J. Curson and R.G. Clark, "Fabrication of quantum wires using scanning probe microscopy", Nano Letters 4, 1969 (2004). [2] S. R. Schofield, N. J. Curson, M. Y. Simmons, F. J. Ruess, T. Hallam, L. Oberbeck and R. G.Clark, "Atomically precise placement of single dopants in silicon", Physical Review Letters 91, 136104 (2003). [3] L. Oberbeck, N. J. Curson, T. Hallam, M. Y. Simmons and R.G. Clark, "Measurement of phosphorus segregation in silicon at the atomic-scale using scanning tunneling microscopy", Appl. Phys. Lett. 83, 1359 (2004).