Abstract Submitted
for the MAR06 Meeting of
The American Physical Society

Silicon surface evolution at high temperature in UHV. VALERIAN IGNATESCU, JACK BLAKELY, Cornell University — The step distribution, associated with the miscut of a Si wafer can be modified by controlled step flow. There are many studies of step-flow dynamics during sublimation or deposition at high temperature. In our group, atomically flat, step-free surfaces were previously obtained over areas of up to 50 by 50 microns by annealing Si samples in UHV. The surface of a normal crystal wafer does not usually show a step-terrace structure. Instead, a Czochralski Si wafer, mirror polished by chemical-mechanical polishing, has an rms roughness of 1-2 nm. A sizable thermal budget has to be used to remove this initial roughness or that induced by reactive ion etching. We report here results of the evolution of step distributions over a range of temperatures. By inducing a temperature gradient on our Si samples we were able to study the stages that occur as the surface transforms towards an atomically flat one. The samples were later reannealed to see the morphological changes that occurred on previously examined regions. We have also investigated the processes of trench formation near the walls of etched craters and of ridge development around the edges of mesas structures.

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Date submitted: 28 Nov 2005 Electronic form version 1.4