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Integration of top-down and bottom-up methods: generating templates for nanowire devices. MATTHEW SHAW, Intel / University College Cork, THOMAS FITZGERALD, UCC, BARBARA KOSMALA, UCC, MICK MORRIS, UCC — Self-assembly can realize spatially controlled nanostructure arrays rivaling the lithography. However, self-assembled constructs to develop nanocircuitry on the macroscopic scale remains distant but combination of lithography and self-assembly might be used for sub-20 nm feature sizes. Spatially constrained block co-polymers can be used to generate these patterns and selective removal of one component can provide 'templates' to generate nanowire arrays. This work focuses on generating nm-size features across a real substrate. We use state of the art lithography to generate sub-μm features and within these generate nm sized co-polymer arrays. Spatial control is determined only by the block size of the co-polymers and not processing variables. Selective 'etching' and phase enhancement techniques were used to provide depth variations across the substrate and form the 'template' for nanowire development. The results of sputtering and electrochemical deposition used to fill the templates are outlined. The results demonstrate an exciting nanofabrication technique for creating high density nanowire arrays for the nanoelectronic industry.

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