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Experimental realization of single electron confinement in an InAs quantum dot G. M. JONES, Department of Electrical and Computer Engineering, University of Maryland, B. H. HU, Department of Electrical and Computer Engineering, University of Maryland, C. H. YANG, Department of Electrical and Computer Engineering, University of Maryland, M. J. YANG, Naval Research Laboratory, Y. B. LYANDA-GELLER, Department of Physics, Purdue University — We demonstrate an enhancement-mode lateral single electron transistor (SET). In contrast to the depletion-mode SETs that reach one-electron regime by expelling electrons from multi-electron QDs, our SET structure uses a single top gate to create two symmetric tunnel barriers and make electrons tunnel into this empty quantum dot one at a time. The sample used in this work to demonstrate this novel SETs concept is an InAs/GaSb composite quantum well, whose bandgap is tunable by the thicknesses of the two QWs and is $\sim 100 \text{meV}$ in our case. Using a gated Hall bar geometry, we show that the device can undergo a transition from hole accumulation to the inversion of electrons. As the widths of the conducting channel and the top gate are reduced to sub-micron, the conductance displays single electron tunneling. The data indicate a 15meV Coulomb charging energy and a 20meV orbital energy spacing, which imply a quantum dot of 20nm in diameter. Combining with the inherent advantage of a large electron g* factor in InAs, our demonstration is significant for solid state implementation of scalable quantum computing.

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