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Metrology for new microelectronic materials. ERIC VOGEL, NIST

Traditional scaling of the CMOS Field-Effect-Transistor (FET) has been the basis of the semiconductor industry for 30 years. The 15 year horizon of the International Technology Roadmap for Semiconductors (ITRS) is reaching a point which "challenges the most optimistic projections for the continued scaling of CMOS (for example, MOSFET channel lengths of roughly 9 nm)." As silicon CMOS technology approaches its limits, new device structures and computational paradigms will be required to replace and augment standard CMOS devices for ULSI circuits. These possible emerging technologies span the realm from transistors made from silicon nanowires to heteroepitaxial layers for spin transistors to devices made from nanoscale molecules. One theme that pervades these seemingly disparate emerging technologies is that the electronic properties of these nanodevices are extremely susceptible to small perturbations in structural and material properties such as dimension, structure, roughness, and defects. The extreme sensitivity of the electronic properties of these devices to their nanoscale physical properties defines a significant need for precise metrology. This talk will provide an overview of emerging devices and materials, and, through example, an overview of the characterization needs for these technologies.