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Observing sub-60mV/dec Switching in Carbon Nanotube Tunneling Field Effect Transistor XINRAN WANG, YUERUI LU, HONGJIE DAI, Stanford University — Single-walled carbon nanotubes (SWNTs) are promising materials for future high performance and nano-electronics due to their high performance of SWNT field effect transistors (FETs) such as Ohmic contact, nearly ballistic transport and ideal switching when integrated with thin high-κmaterials. Yet the ideal structure for SWNT transistors is still unclear due to non-ideal behaviors when transistor size is scaled down. Recently, PIN structure is proposed as an ultimate structure for SWNT-FETs on a single device level. In this work, SWNT-FETs with n- and p- doped source and drain and ultra thin high-κgate dielectrics is first experimentally fabricated and characterized. This novel tunneling transistor structure is based on quantum mechanical band-to-band tunneling current between conduction and valence band of semiconducting SWNTs as opposed to the conventional Schottky type devices. Sub-60mV/dec subthreshold slope (SS) is observed reliably in our PIN transistors for $\sim$3 orders of current level on both p- and n- channels in transfer characteristics. The previously reported charge pile-up effect in SWNT-FETs is suppressed in our devices. By comparing the performance of PIN transistors with PIP MOSFETs, we find that PIN could offer lower off-state current and better on/off ratio while maintaining a decent on-state current and thus is suited for low power dissipation applications.

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