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First-principles study of direct electron tunneling through ultra-thin SiO_2 layers JOONGOO KANG, K.J. CHANG, Department of Physics, Korea Advanced Institute of Science and Technology, South Korea, Y.-H. KIM, Department of Materials Science and Engineering, University of Seoul, South Korea —
As the size of metal-oxide-semiconductor devices is scaled down to the sub-10-nm regime, the thickness of SiO_2 insulating layers reaches the range of 1-2 nm. Then, gate leakage current is unavoidable due to direct tunneling of electrons. In this work, we study the electron tunneling current through thin gate oxide layers for various Si(100)/SiO_2 interface models, which have different oxide thicknesses and crystal phases. We use a combined approach of the local-density-functional approximation and the matrix Green's function method. We test oxide layers in the α-quartz, tridymite, and amorphous structures, which are sandwiched between two Si(100) electrodes. We find that Si induced gap states result from a decay of the silicon valence (conduction) band wave functions into the oxide region. The gate leakage current between two p+ Si electrodes is exponentially reduced as the oxide thickness increases, with the almost same decay rate of -1 decade/0.2 nm, regardless of the structure of oxide layers. We also find that the gate leakage current is affected by introducing interface roughness and oxygen vacancies in the oxide.

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