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Nanowire Non-volatile Memory with Silicon Nitride Charge Trapping Layer QILIANG LI[1], XIAOXIAO ZHU, D.E. IOANNOU[2], J.S. SUEHLE, C.A. RICHTER, NIST — We present the fabrication and characterization of Si nanowire field effect transistors with silicon nitride as a charge trapping layer for non-volatile memory application. The Si nanowires were grown by chemical vapor deposition on defined location on a 60 nm Si nitride which was deposited on a 20 nm thermal grown oxide (blocking oxide). The source/drain electrodes were formed by using photolithographic alignment and metal lift-off processes. The nanowires were then covered with sputtering oxide at room temperature to be isolated from the external environment. We have observed a large threshold voltage shift window (8 V) at 10 V write/erase voltage and non-volatile on/off current states, which is attributed to the small radius ($\sim$ 10 nm) and intrinsic doping of the Si nanowire. The dynamics of the nanowire/nitride charge exchange, and its effect on threshold voltage and memory retention have been studied.

[1]Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899, USA
[2]Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030

Qiliang Li

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